Performance Analysis and Development of Self- Consistent Model of Carbon Nanotube Field Effect Transistor (CNTFET)

Ashraful Haider Chowdhury, Nargis Akhter and Asif Al Faisal

The rising demand for ultra high speed processors has made the transistor scaling a challenging issue in present days. As Si-MOSFET scaling is moving towards its limiting value, ballistic CNTFET has become the most likely component to replace the Si-MOSFET transistors. In this paper we have analyzed several performance criteria for CNTFET over traditional Si-MOSFET. We have modelled CNTFET device based on a solution to Poisson's equation that connects the electrostatic potential in the device to charge induced in the CNT and charge distribution for the device is found by solving Schrödinger's equation. The paper proposes CNTFET is the device of choice for next generation VLSI chips with its high-performance and smaller dimensions.

Index Terms—CNT, CNTFET, Si-MOSFET, Self Consistent Model**,** Schottky barrier.

I. INTRODUCTION

Transistors in an integrated circuit has always obeyed the "Moore's law". It states that the number of transistors that can be placed in an integrated circuit has doubled approximately every two years. Nanoscale field effect transistors suffer from short channel effects such as direct tunnelling from source to drain and increase in gate-leakage current. These effects have posed severe problems for smaller sized transistors. Recent years MOSFET scaling has reached its limiting value and thus new alternatives are coming up to overcome these limitations. Semiconducting carbon nanotubes (CNTs) because of their properties like large mean free path, excellent carrier mobility and ballistic conduction have made them as an ideal material for transistor channel in replacement for silicon. CNTs suppress the short channel effects in transistor devices. CNTs are purely one dimensional device and they can be used to achieve ultra high speed ballistic CNTFET (carbon nanotube field effect transistor).CNTFETs works in the terahertz regime in comparison with that of silicon MOSFETs. Transistors other than the MOSFETs can be grouped into two categories[1]-a. Quantum effect and single electron solid devices and b. molecular electronic devices. Carbon nanotube based transistors (CNTFET) are the most promising molecular electronic devices. Recent years CNTFETs are the most likely research topic in the nanoscale technology and ideas are generating for creating nanodevices.

EECE Dept, Military Institute of Science and Technology
Mirpur cantonment, Dhaka , Bangladesh
ashrafulhaider@rocketmail.com, Phone number: **01916758546**

II. NANO-STRUCTURE DEVICES

Nanoscience research focuses primarily on creating the technology necessary for the development of nanodevices. Thus it gave birth to Carbon Nanotube and Carbon Nanotube Field Effect Transistor.

A. Carbon Nanotube

Since carbon nanotubes discovery in 1991 by Iijima while perfoming experiments on carbonium, they have been of great interest, both from a fundamental point of view and for future applications. The most eye-catching features of these structures are their electronic, mechanical, optical and chemical characteristics, which leads to the future applications in nanoelectronics. Carbon nanotubes are allotropes of carbon which belongs to the fullerenes family and are sheets of graphene rolled in the shape of a tube having a large length to diameter (132000000:1) ratio (lengths are in micro range & diameters in nm range).

For this unique property CNTs are 1D materials [2].it can be classified into SWCNT(single walled carbon nanotube) & MWCNT (multi walled carbon nanotube).

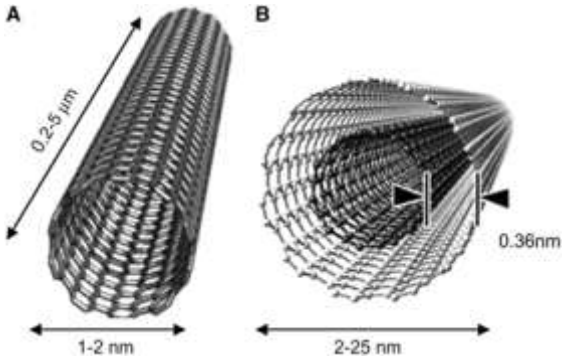

Fig. 1 Carbon nanotube (CNT) structure (A) SWCNT (B) MWCNT.

Depending on the arrangement of carbon atoms & how the graphene sheet is rolled up SWCNTs can be of metallic or semiconducting nature. On the basis of chirality, bandgap of CNTs can be varied to large extent and thus it can be either metal or semiconductor. Diameter of CNTs can be calculated as

$$d = (\frac{a}{\pi})\sqrt{m^2 + mn + n^2} \qquad (1)$$

The way the graphene sheet is rolled up can be represented by indices (m,n) & a=lattice constant (.246). If m=0 then zigzag nanotube, n=m armchair CNTs and otherwise chiral. Following equations present whether CNTs will be metallic or semiconducting [3]

n - m = 3i (i=0,1,2,3…)	metallic CNT
n - m ≠ 3i	semiconducting CNTs

Fig. 2 a) Schottky Barrier CNTFET, b) MOSFET-like CNTFET.

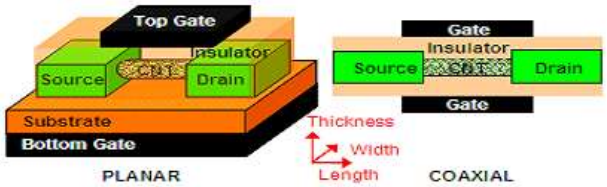

Fig. 3 CNTFET structure: (a) Planar, (b) Coaxial.

B. CNT Field Effect Transistor

CNTs are very attractive for nanoelectronic applications and can be used to achieve high speed ballistic carbon nanotube field effect transistors (CNTFETs). Theoretically, CNTFETs could reach a higher frequency domain (terahertz regime) than conventional semiconductor technologies. Mainly two types of semiconducting CNTFETs are there classified on the basis of material composition: a) SB-CNTFET and b) MOS-CNTFET.

SB-CNTFET (Fig. 2(a)) works on the principle of direct tunnelling through a Schottky barrier at the source-channel junction. The barrier width is modulated when gate voltage is applied and thus the transconductance of the device becomes dependent on the gate voltage. To overcome these problems associated with the SB CNTFETs, there have been attempts to develop CNTFETs which would behave like normal MOSFETs (Fig. 2(b)). In this MOSFET-like device, the source and drain regions are heavily doped and the CNTFET operates on the principle of barrier-height modulation by application of the gate potential. This will give a higher on-current as it is limited by the amount of gate-induced charge in the channel. Ambipolarity seems to occur in SB-CNTFET, to overcome a new has been developed known as SO-CNTFET. Schottky barrier is formed at source-channel junction and Ohmic contact is formed at drain-channel junction.

1) Planar and Coaxial CNTFET:

Conventional CNTFET and Tunnelling CNTFET are of planer structure. [Fig. 3(a)]. Besides these planar structures one more structure is also developed which is known as coaxially gated CNTFET [Fig. 3(b)]. [4]

III. CNTFET OVER SI-MOSFET

Assessment of CNTFET with respect to Si-MOSFET is studied from different viewpoints. A brief comparison is given in the following table why CNTFET is more preferred than Si-MOSFET for next generation transistors.

TABLE I
Assessment of CNTFET vs. Si-MOSFET

Property	Brief comparison
Channel length	Typically in CNTFET it is 10 nm while in Si-MOSFET it is 22 nm [5] (up to year 2009). Smaller channel length results in better carrier transport. Smaller channel is a vital factor for next generation Moore's law.
Carrier mobility	Due to high-κ gate dielectrics of CNTFET carrier mobility becomes higher than that of Si-MOSFET [6]. Carrier velocity, which is dependent on mobility, almost doubles in CNTFET.
Ballistic conduction	Is possible in CNTFET as the mean free path of electron is larger than the channel length of CNTFET. Only back and front side scattering of carrier occurs.[7] While in traditional MOSFET boundary scattering occurs. This results in better conduction and low leakage in CNTFET.
Threshold voltage	Lower in CNTFET which causes faster switching and low power dissipation.
Gate capacitance	Higher in CNTFET. In p-CNTFET ~1500 A/m of the on-current per unit width at a gate overdrive of 0.6 V is produced while traditional p-MOSFET produces ~500 A/m at the same gate voltage.[8] Faster switching is possible.
Contact resistance	Modulation of contact resistance increases the switching capacity of CNTFET while in Si-MOSFET switching occurs by altering channel resistance.
Transconductance	Due to better control over the gate, transconductance is four times higher in CNTFET. As a consequence, small change in voltage gives large current.
Dielectric constant	Due to higher dielectric constant [4], tunnelling effect decreases, which cause low leakage.
Subthreshold slope	In Si-MOSFET, is about 60 mV/decade but in CNTFET it can be made higher to an optimized value which results in lower power dissipation in off-devices.[9]
Heat dissipation	The self-heating effect is much less severe in a CNTFET. Heat dissipation is non-uniform through the channel with highest value appearing at the source and drain sides of the channel.[10] The temperature rise has a relatively small effect on the I-V characteristics compared to Si-MOSFET.

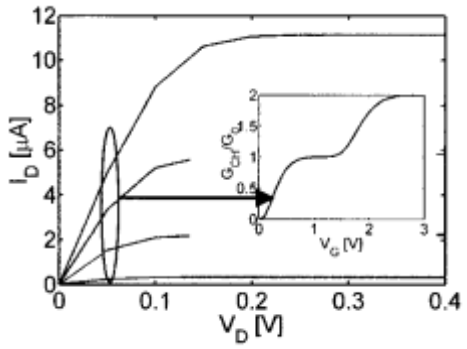

Fig. 4 The computed ID vs VD characteristic with gate bias as a parameter (VG=0.1–0.4 V, 0.1 V/step.) The inset shows the quantized channel conductance vs. gate voltage at T=300 K. The normalization conductance G0=4e2/h, where e is the electron charge and h the Planck constant

As the conductance curve is quantized in CNTFET [11], I_D will not be high (logic 1) if input voltage V_D is not sufficiently high. Thus the effect of noise is less and consequently Bit Error Rate lowers. So, CNTFET should be the device of choice for digital communication circuit.

IV. SELF CONSISTENT SOLUTION FOR CNTFET- PROPOSED

With the advancement of semiconductor technology, device dimensions are entering into the nanoscale regime; quantum mechanical effects are playing a growing role in device operations and performance. So quantum mechanical model connects Schrödinger and Poisson equations which are solved self consistently [12]. The Schrödinger equation is solved under the effective mass approximation [13]. The boundary condition of the Schrödinger and Poisson equations is also a critical issue. To calculate quantum mechanical charge distribution in CNTFET device incorporating the wave function penetration effect within the oxide layer of MOS devices an open boundary condition is a must for the solution of Schrödinger equation. In this section, the solution procedure is performed for a dual MOS-CNTFET structure shown in Fig. (5). COMSOL with MATLAB has been used as the Partial Differential Eqn. (PDE) solver (suitable for linear or nearly linear problems), for the self-consistent solution. The classical PDEs coefficient form in multi-physics mode is used for the Poisson and Schrödinger equation. Poisson equation in coefficient form is given in COMSOL as:

$$-\nabla(c\nabla u) = f \tag{2}$$

Where *c, u* and *f* indicate permittivity of the sub domain, electrostatic potential and charge density respectively.

Assuming *f* =0, we get the trial potential *u*(z) (Fig. 6). z signifies position along gate to gate. Schrödinger equation in coefficient form is defined in COMSOL as:

$$-\nabla(c\nabla u)+au=\lambda u \qquad (3)$$

Where a, u and λ are electrostatic potential, eigen function and Eigen energies respectively. Using relevant parameters of effective mass Schrödinger equation for one dimensional MOS structure quantum well (3) can be written as-

$$[-\frac{\hbar^2}{2m^*}\frac{d^2}{dz^2}+v(z)]\psi_{ij}(z)=E_{ij}\psi_{ij}(z) \qquad (4)$$

E_{ij} and ψ_{ij} are the eigen value and the eigen function of an electron in the *j*th energy level of the *i*th valley, which are obtained as a solution of the one-dimensional Schrödinger equation.*u*(z) from (2) is used as *v*(z) in (4) to solve Schrödinger equation in order to get wave function ψ_{ij}(z). The electron concentration *n*(z) is obtained for n-MOS structure according to the following expression:

$$n(z)=\sum_{ij}N_{ij}\left|\psi_{ij}(z)\right|^2 \qquad (5)$$

Where Nij is the carrier concentration in the jth subband of the ith valley.

V. PROPOSED MODEL FOR CNTFET

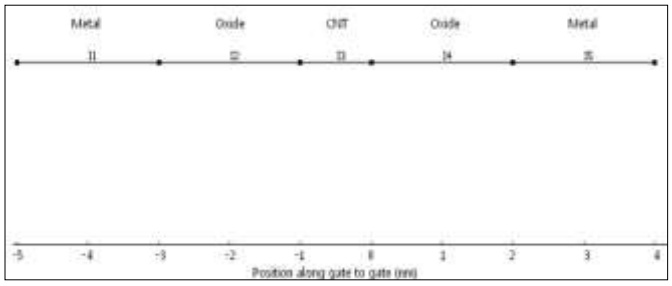

Fig. 5 1D geometry of Double Gate MOS-CNTFET structure.

Parameters used in CNTFET modelling are given below:

TABLE II
MODEL SPECIFICATION

Material	Region in fig (5)	Parameter	Value
Aluminium (gate metal)	I1, I5	Surface charge density	0
		Electron effective mass	$0.97m_e$
HfO_2 (oxide)	I2, I4	Relative permittivity	16
		Electron effective mass	$0.2m_e$
CNT (11,3) (channel)	I3	Electron effective mass	$0.255m_e$
		Surface charge density	6.034×10^{14} cm^{-3}

In fig (5), Dirichlet boundary condition for boundary points 1, 2, 5, 6 and Neumann boundary condition for 3, 4 interfaces are used for Poisson equation. A discontinuous electric field boundary condition can be easily set with Neumann boundary condition in COMSOL. Then the charge density profile *n*(z) is determined from (5) by solving (3) using COMSOLE eigen-value solver with Neumann boundary condition (needed for open boundary condition to consider penetration effect).

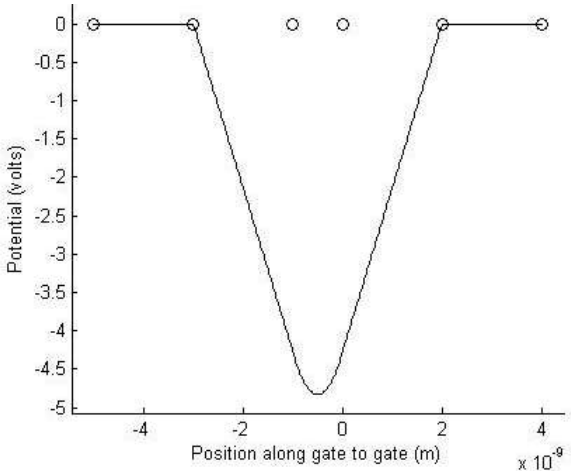

Fig.6 Trial potential from full depletion approximation.

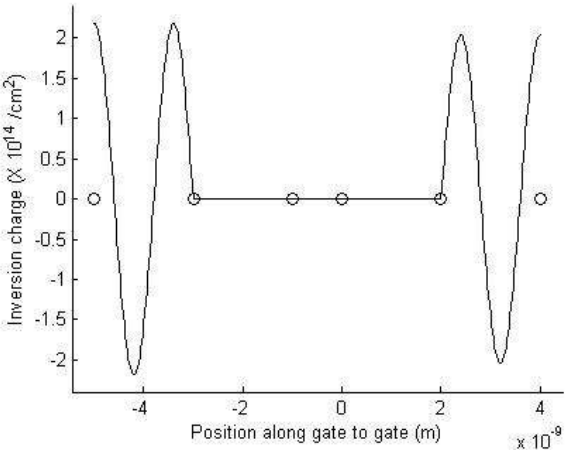

Fig. 7 Inversion charge density as a function of position.

VI. SCOPE OF FUTURE WORKS

The carbon nanotube degrades in a few days when exposed to oxygen. Carbon nanotubes have shown reliability issues when operated under high electric field or temperature gradients. Avalanche breakdown occurs in semiconducting CNT and joule breakdown in metallic CNT [14]. There has been several works done on passivating the nanotubes with different polymers and increasing their lifetime [15]. Multiwall CNT can also serve to increase the lifetime significantly. The most desirable future work involved in CNTFETs will be adding effects external to the inner CNT transistor like the Schottky barrier between the CNT and metal contacts, multiple CNTs at a single gate, channel fringe capacitances, parasitic source/drain resistance, and series resistance due to the scattering effects [16].

VII. CONCLUSIONS

This paper reviews different types of CNTFET which are the promising candidates for next generation MOS transistors and also gives an insight to performance analysis of CNTFET over Si-MOSFET. We ascertained that CNTFET gives substantially higher performance than traditional transistors. We have also proposed an improved and numerically efficient self-consistent model for CNTFET. Our self-consistent model may be used for simulating many devices.

REFERENCES

[1] F. Prégaldiny, C. Lallement, J.-B. Kammerer, "*Design-oriented compact models for CNTFETs*," Proc. DTIS 2006, 5-7 September, 2006, Tunis, Tunisia, in press.

[2] Wang, X.; Li, Qunqing; Xie, Jing; Jin, Zhong; Wang, Jinyong; Li, Yan; Jiang, Kaili; Fan, Shoushan, "*Fabrication of Ultralong and Electrically Uniform Single-Walled Carbon Nanotubes on Clean Substrates*". *Nano Letters* 9 (9): 3137–3141, 2009

[3] Mintmire, J.W.; Dunlap, B.I.; White, C.T., "*Are Fullerene Tubules Metallic?*". *Phys. Rev. Lett.* 68 (5): 631–634. 1992

[4] Rasmita Sahoo and R. R. Mishra, *"Simulations of Carbon Nanotube Field Effect Transistors"*, International Journal of Electronic Engineering Research, ISSN 0975- 6450 Volume 1 Number 2 pp. 117–125, 2009

[5] International technology roadmap for semiconductors,2009 Edition

[6] Zahra Arefinia; Ali A. Orouji *"Investigation of the novel attributes of a carbon nanotube FET with high-k gate dielectrics",* Physica E 40 3068– 3071; 2008.

[7] Wong, H. -S. Philip, and Deji ,. Akinwande. "*Carbon Nanotube and Graphene Device Physics*", Cambridge UP, 2011. Print.

[8] Jing Guo; Datta, S.; Lundstrom, M.; Brink, M.; McEuen, P.; Javey, A.;Hongjie Dai; Hyoungsub Kim et al. ,` *Assessment of silicon MOS and carbon nanotube FET performance limits using a general theory of ballistic transistors",*2002

[9] R. V. Seidel,* A. P. Graham, J. Kretz, B. Rajasekharan, G. S. Duesberg, M. Liebau, E. Unger, F. Kreupl, and W. Hoenlein *"Sub 20 nm Short Channel Carbon Nanotube Transistors",* Infineon Technologies AG, Corporate Research, 81730 Munich, Germany.

[10] Ouyang, Yijian; Guo, Jing, "*Heat dissipation in carbon nanotube transistors*". *Applied Physics Letters* 89 (18): 183122, 2006

[11] Jing Guo, Mark Lundstrom, and Supriyo Datta, "*Performance projections for ballistic carbon nanotube field-effect transistors*", Applied physics letters, volume 80, number 17, 29 April 2002

[12] Ason Paul Clifford, "*A self consistent numerical model for bipolar transport in carbon in carbon nanotube field effect transistors*", December 2003

[13] Jose Mauricio Marulanda Prado *"Current transport modeling of carbon nanotube field effect transistors for analysis and design of integrated circuits",* August 2008

[14] Pop, Eric; Dutta, Sumit; Estrada, David; Liao, Albert, "*Avalanche, joule breakdown and hysteresis in carbon nanotube transistors*", pp. 405, 2009

[15] L. Crockett, *"Carbon Nanotube Transistor Fabrication and Reliability Characterization"*, Intel

[16] Kazmierski, Tom J.; Zhou, Dafeng; Al-Hashimi, Bashir M.; Ashburn, Peter *"Numerically Efficient Modeling of CNT Transistors with Ballistic and Nonballistic Effects for Circuit Simulation"*, IEEE Transactions on Nanotechnology 9: 99. , 2010